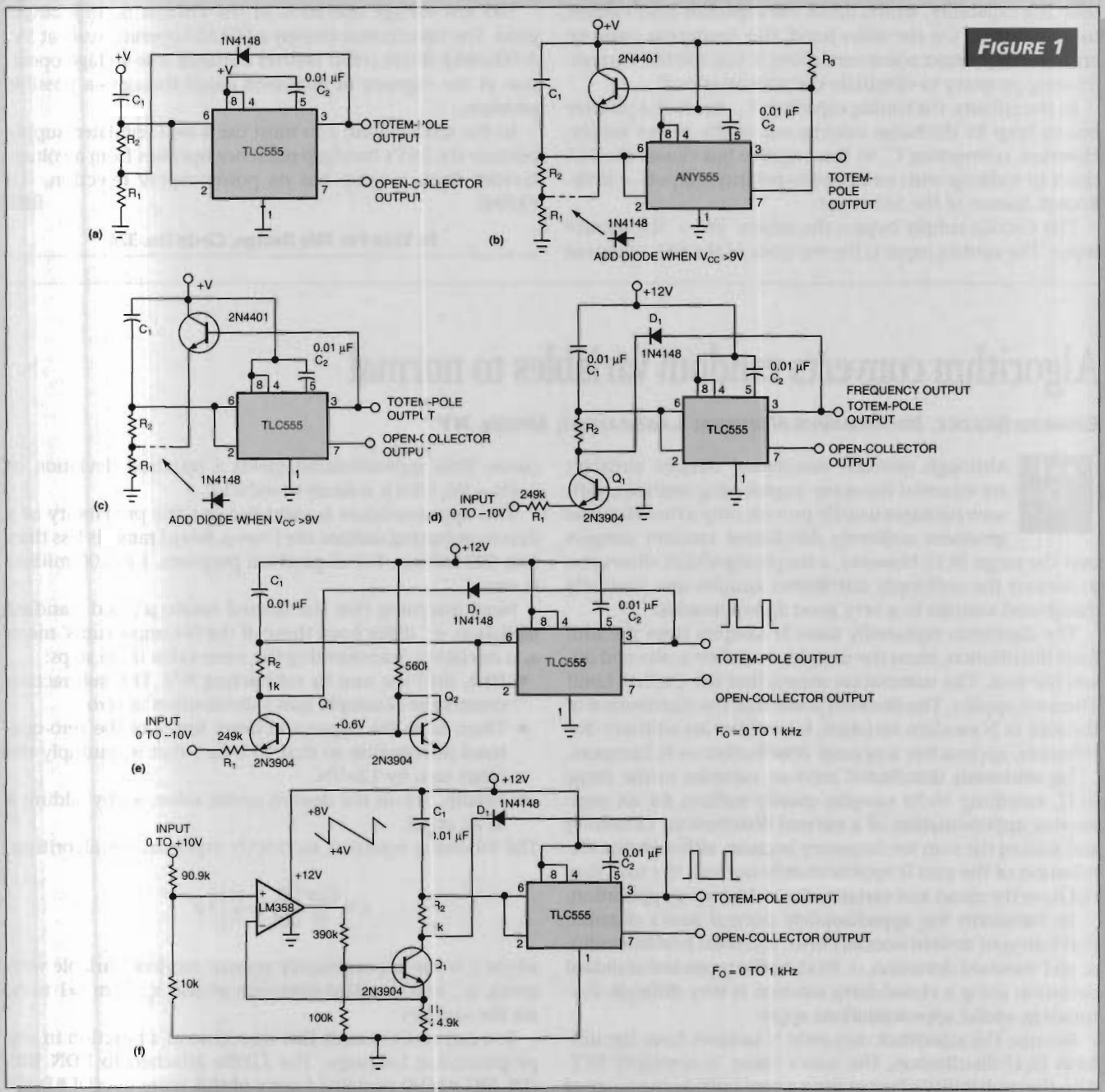
Old-dog 555 learns six new tricks

JAMES KEITH, IMD FINCOR ELECTRONICS DIVISION, YORK, PA

The circuits in Fig 1 invert the ubiquitous 555 timer's operation. The circuits' output polarities are the inverse of conventional 555 timers'. The circuits' output duty cycle is exactly 50%. Further, you have a choice of open-collector or totem-pole output—or both. And you can feed the timing capacitor from a negative current source referenced to the circuit's common.

I recommend the Texas Instruments TLC555, but any 555



You can configure an "inverted" CMOS 555 timer as a free-running oscillator (a), an inverted bipolar 555 with active reset (b), an inverted CMOS 555 with active reset (c), a simple VCO (d), an improved version of the VCO (e), and a VCO sporting an amplified current source (f).

timer should work. The TLC555 has the advantage of being CMOS. Its low power consumption does not introduce switching spikes into the power supply. The TLC555's output also tends to saturate better in the positive direction than devices from other CMOS 555-timer vendors. This feature suits the TI device better for this application.

One disadvantage of the TI device is its limited output-sourcing capability, which limits the capacitor-reset current to 10 mA max. On the other hand, this limitation could be an advantage under some conditions if you use the current-limiting property to eliminate the reset-resistor, R_2.

In the circuits, the timing capacitor, C_1, ties to the positive bus to keep its discharge current out of the power supply. However, connecting C_1 to the negative bus causes the 555 timer to wake up with an opposite-polarity output—a little-known feature of the 555 timer.

The circuits simply bypass the timers' pin 5, the control input. The control input is the top node of the 555's internal voltage divider. In these circuits, bypassing this node to V_{CC} via C_2 stabilizes the devices' upper threshold. But the lower threshold is at the mercy of the power-supply bus. Therefore, I recommend bypassing the power supply with a healthy sized capacitor to minimize jitter induced in the 555's lower threshold. This extra capacitor is one disadvantage of these configurations.

The low-voltage operation of the circuits is surprisingly good. The circuits that employ a TCL555 operate easily at 5V. A Schottky diode could further enhance low-voltage operation at the expense of increased diode leakage—a possible problem.

In the sixth circuit, you must use a well-regulated supply because the 555's bandgap reference operates from a voltage divider. Such a setup has *no* power-supply rejection. (DI #1694) EDN

To Vote For This Design, Circle No. 324

Algorithm converts random variables to normal

EDWARD BEADLE, BROOKHAVEN NATIONAL LABORATORY, UPTON, NY

BBS

Although *normally* distributed random variables are essential for many engineering analyses, software packages usually provide only a function that generates *uniformly* distributed random samples over the range [0,1]. However, a simple algorithm allows you to convert the uniformly distributed samples into normally distributed samples to a very good approximation.

The algorithm repeatedly takes N samples from the uniform distribution, sums the samples, and then scales and offsets the sum. The summation means that the Central Limit Theorem applies. The theorem states that the distribution of the sum of N random variables, taken from an arbitrary distribution, approaches a normal distribution as N increases.

For uniformly distributed random variables in the range [0,1], summing N=20 samples usually suffices for an engineering approximation of a normal distribution. Offsetting and scaling the sum are necessary because, although the distribution of the sum is approximately normal, the sum may not have the mean and variance desired for your application.

To transform the approximately normal sum's distribution into your desired normal curve, you must find the mean, μ, and standard deviation, σ. Finding the mean and standard deviation using a closed-form solution is very difficult. Fortunately, useful approximations apply.

Because the algorithm uses only N samples from the uniform [0,1] distribution, the sum's mean is obviously N/2. Also the probability of generating a sum outside the range of [0,N] is exactly zero. So, to determine the standard deviation of the approximately normal sum's distribution, the algorithm equates the maximum possible value of the sum of N samples to the $6\sigma+\mu$, or "six sigma," point on the normal curve. This approximation yields a standard deviation of $\sigma=(N-\mu)/6$, which reduces to $\sigma=N/12$.

This approximation is valid because the probability of a datum occurring outside the $[-6\sigma-\mu,6\sigma+\mu]$ range is less than 1 in 500 million. For all practical purposes, 1 in 500 million is zero.

Next, assuming that the desired mean, μ', and standard deviation, σ', differ from those of the N-sample sums' mean and deviation, transforming the sums takes three steps:

- First, shift the sum by subtracting N/2. This subtraction centers the N-sample sum's distribution at zero.
- Then, scale the upper and lower limits of the zero-centered distribution so that $N/2=6\sigma'$; that is, multiply the offset sum by $12\sigma'/N$.
- Finally, obtain the desired center value, σ', by adding it as an offset.

The following equation succinctly expresses the algorithm:

$$z = \frac{12\sigma'}{N}\left(\sum_{i=1}^{N} x_i - \frac{N}{2}\right) + \mu'$$

where z is the approximately normal random variable with mean, μ', and standard deviation σ' and x_i, from i=1 to N, are the samples.

You can easily encode this algorithm as a function in any programming language. The ZIPfile attached to **EDN BBS /DI_SIG #1590** contains a copy of this write-up. (DI #1690) EDN

To Vote For This Design, Circle No. 325

Two cores marry, make swinging choke

VINCENT SPATARO, GEC MARCONI ELECTRONIC SYSTEMS CORP, WAYNE, NJ

BBS

Designing an output choke for a switch-mode power supply that must operate over large load variations can be problematic. If you design the inductor for the maximum load the power converter will see, the inductance will be below the critical inductance required at light load. This inadequate inductance will cause the voltage on the output capacitor to peak up, resulting in increased ripple on the output.

If, on the other hand, you design for the much larger value of inductance required at light load, your inductor will be overspecified for the nominal load and will be too large physically.

One solution is to add a bleeder resistor on the output of the supply to keep a minimum amount of current flowing at all times. This "fix" is not very efficient and often is an unacceptable solution, especially for battery-powered circuits.

A better solution is to use a swinging choke, which exhibits a large inductance at light load and a progressively smaller inductance as the load increases. The size of the swinging choke is considerably smaller than an overspecified conventional choke. And a swinging choke is more efficient than a bleeder resistor.

A new series of gapped ferrite toroids from Ferrite Specialties Inc (Conshohocken, PA) makes swinging-choke design easy. You wind together a gapped ferrite toroid and an ungapped ferrite having the same form factor. The ungapped ferrite provides high inductance at light load but saturates at less than full load current. The gapped ferrite core provides much lower inductance at light load but doesn't saturate, providing a working inductance at full load. The result of the series combination of the two inductors is a single compact structure that doesn't require a coil bobbin and is easy to construct and mount. Fig 1a offers a schematic representation of the swinging choke; Fig 1b shows the mechanical construction.

As a design example, assume you want a 12.5-μH choke that operates at a nominal load current of 2A. This specification requires 20 turns of #18 AWG wire on a gapped Ferrite Specialties PGTX221406A36 core. This core has a gap l_G=0.0138 cm, a cross-sectional area A_E=0.259 cm, and an A_L=36 mH/1000T. At the nominal operating current of 2A, this core sees a flux density of

$$B = \left[\frac{0.4\pi LI^2}{A_E l_G} 10^8\right]^{\frac{1}{2}} = 1.32 \text{ kG}.$$

At this value for flux density, the core is operating far from saturation at nominal current and has plenty of design margin.

To design the high-inductance portion of the choke for the lightly loaded condition, use a standard ungapped ferrite core, a Philips 846T250-3C85. This core has an A_L=1220, μ=2000, and a magnetic path length l_c=5.42 cm. For the same number of turns, N, the inductance of this core is

$$L(\mu H) = \frac{N^2 A_L}{10^3} = 488\ \mu H.$$

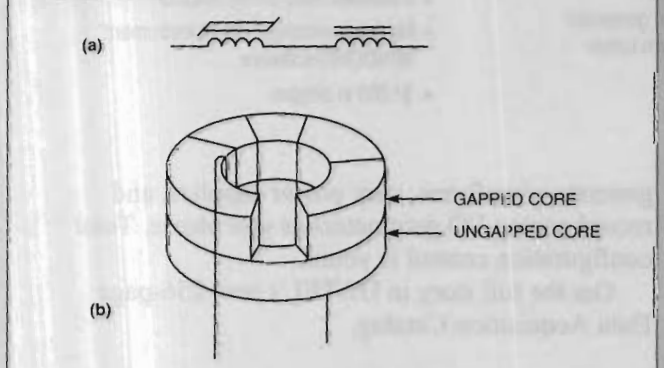
This core fully saturates at approximately B=5 kG. The current at this flux density is

$$I = \frac{Bl_C}{0.4\pi\mu N} = 0.54A.$$

The total inductance of the core is the series combination of the gapped and ungapped inductors. At low current, the ungapped core dominates, producing a very large inductance. At 0.54A, however, the ungapped core saturates, reducing its inductance (essentially) to zero. The ungapped core then dominates, producing a working inductance at the full load current of 2A. The ZIP file attached to EDN BBS /DI_SIG #1692 contains a copy of this write-up. (DI #1692)

EDN

FIGURE 1



Winding an ungapped core together with a gapped core (a) forms a swinging choke (b) having ideal properties for the output choke of a switching power supply.

Spice model simulates broadband transformer

MICHAEL STEFFES, COMLINEAR CORP, FORT COLLINS, CO

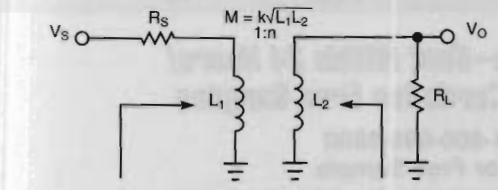
BBS

The approximate model in Fig 1 makes it easier to include high-frequency transformers in a Spice simulation. Broadband pulse transformers are widely used to transform impedance levels as a noise-reduction or source-matching technique. Fig 1 includes the physical model and the key performance equations. The model shows the transformer providing a voltage gain from V_S to V_O, an input impedance of R_L/n^2, and an output impedance of n^2R_S.

To simulate the transformer, the Spice simulation requires L_1, L_2, and k as inputs. However, transformer manufacturers typically specify only an impedance ratio (n^2) and the two –3-dB frequencies of the transformer's bandpass response. If the passband is greater than two decades wide, which translates into k>0.98, the following Laplace bandpass transfer function approximates the frequency response for the model:

$$\frac{V_O}{V_S} \approx \frac{s\dfrac{R_{L/n}}{(1-k^2)L_1}}{\left(s+\dfrac{R_S+R_{L/n^2}}{(1-k^2)L_1}\right)\left(s+\dfrac{R_S \| \left(R_{L/n^2}\right)}{k^2L_1}\right)}, \quad (1)$$

FIGURE 1



MIDBAND $Z_I = \frac{R_L}{n^2}$ MIDBAND $Z_O = n^2R_S$

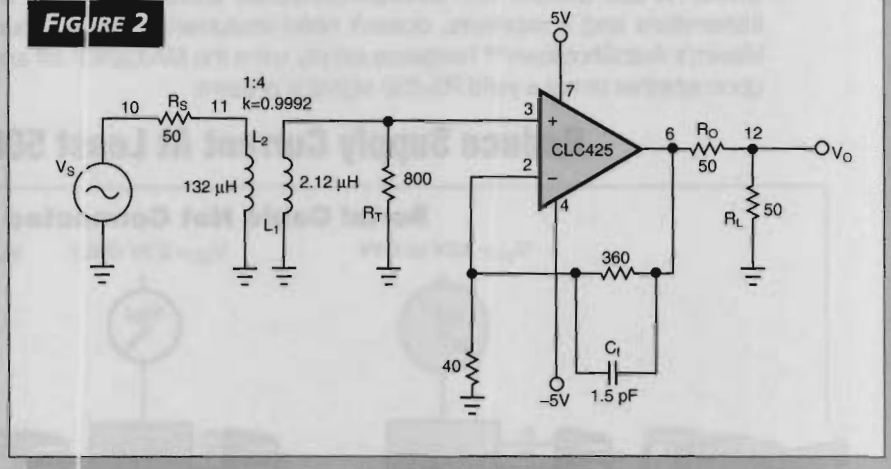
MIDBAND GAIN = $\frac{V_O}{V_S} = n\frac{R_L}{R_L+n^2R_S}$

M=MUTUAL INDUCTANCE; k=COUPLING COEFFICIENT;

n=TURNS RATIO; $n=\frac{N_2}{N_1}=\sqrt{\frac{L_2}{L_1}}$.

Using this approximate model of a high-frequency transformer, you can easily include transformers in a Spice simulation.

FIGURE 2



This simulation test circuit places the transformer model in front of an op amp, a configuration that reduces the op amp's noise figure.

where the left denominator term determines the low-frequency cutoff of $2\pi f_L$ and the right denominator term determines the high-frequency cutoff of $2\pi f_H$. Manufacturers usually specify the –3-dB frequencies, f_L and f_H, of broadband pulse transformers with R_S=50Ω and $R_L=n^2R_S$. You can solve Eq 1 for the three required Spice model parameters as follows:

$$L_1 = \frac{R_S/2}{2\pi f_L} = \frac{\dfrac{R_L}{2}\dfrac{1}{n^2}}{2\pi f_L} \Big| R_S = 50\Omega,\ R_L = R_S n^2$$

$$L_2 = n^2L_1 = \frac{R_L/2}{2\pi f_L} \Big| R_S = 50\Omega,\ R_L = R_S n^2$$

$$k = \sqrt{\frac{1}{1+4\dfrac{f_L}{f_H}}}.$$

To illustrate how this model works, consider using a 1:4 transformer in front of a low-noise op amp to reduce its noise figure. The specifications for an RF Prime (Sacramento, CA, (916) 368-4400)) RFTM-16 transformer indicate an impedance ratio of 16 (n=4) and –3-dB frequencies of 30 kHz and 75 MHz. The three input parameters are as follows:

$$L_1 = \frac{25\Omega}{2\pi(30\ \text{kHz})} = 132\ \mu\text{H}$$

$$L_2 = \frac{400\Omega}{2\pi(30\,\text{kHz})} = 2.12\ \text{mH}$$

$$k = \sqrt{\frac{1}{1+4\left(\dfrac{30\ \text{kHz}}{75\ \text{MHz}}\right)}} = 0.9992.$$

You can now use the transformer model along with the op amp's macromodel to develop a full simulation for the test circuit in **Fig 2.** This circuit provides a good 50Ω input- and output-impedance match, a midband gain of +10 (20 dB) from the source to the matched load, and an input-noise figure that has been reduced from 9.5 dB for just the op amp to 4.2 dB with the input transformer.

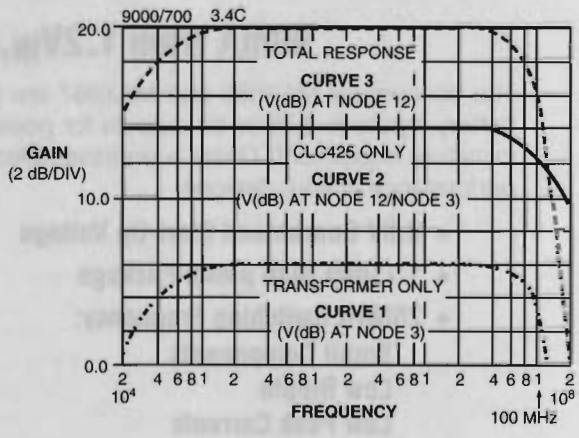
Curve 1 in **Fig 3** shows the response of the transformer only. With $R_T=n^2R_S$, the circuit attenuates V_i by one-half to the input of the transformer and then provides a gain of n to the secondary side. The result is a net gain of +2 from the source to the input of the op amp. Curve 1 shows this midband gain and the correct low-frequency cutoff and also what appears to be second-order high-frequency roll-off. The op amp's input capacitance causes this roll-off, and removing the op amp shows exactly the desired 75-MHz single-pole roll-off for the transformer by itself. Curve 2 shows the response of the op amp alone. C_F intentionally bandlimits the op amp's response to reduce high-frequency noise at the output.

Curve 3 is the total response from the source to the load showing the desired 20-dB gain with approximately the same frequency response as the transformer.

Ed Note: The author thanks Paul Clark at RF Prime for his suggestion in applying high-frequency transformers and for verifying the simplified model shown here. (DI #1681) EDN

To Vote For This Design, Circle No. 327

FIGURE 3



Three simulated curves of the transformer's response (Curve 1), the op amp's response (Curve 2), and the total response (Curve 3) confirm that this model produces the desired 20-dB gain with approximately the same frequency response as the transformer.

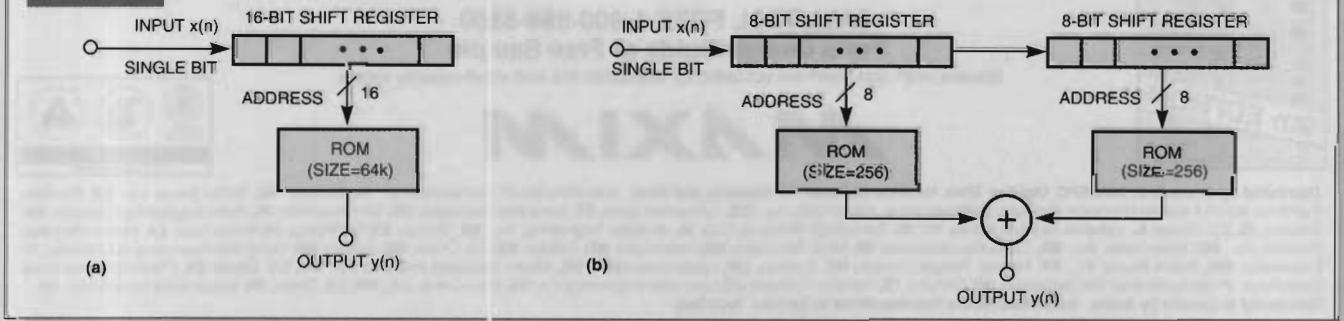
FIR-filter scheme saves ROM storage space

CA JALALUDEEN, DEFENCE R&D ORGANISATION, KOCHI, KERALA, INDIA

You can easily implement single-bit FIR filters using ROM look-up tables, which allows you to avoid costly multiplier accumulators. Unfortunately, as filter order increases, so does the size of the ROM. **Fig 1** shows how you can reduce the storage requirement for larger-order filters.

The following difference equation defines an N-tap FIR fil-

FIGURE 1



The direct implementation of an single-bit input FIR filter (a) requires a huge ROM as filter order increases. Splitting the summation in two or more partial sums (b) reduces ROM's storage requirements.